L Number	Hits	Search Text	DB	Time stamp
1	265	double near5 fifo	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:14
2	1	(arbitrat$4 near5 request$3) same (double near5 fifo)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:16
3	715	(arbitrat$4 near5 request$3) same switch$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:17
4	1	(double near5 fifo) and ((arbitrat$4 near5 request$3) same switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:34
5	59	central same ((arbitrat$4 near5 request$3) same switch$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/05 12:35

PGPUB-DOCUMENT-NUMBER: 20010023469

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010023469 A1

TITLE: Distributed type input buffer switch system for transmitting arbitration information efficiently and method for processing input data using the same

PUBLICATION-DATE: September 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Jeong, Gab-Joong	Taejon		KR
Lee, Jung-Hee	Taejon		KR
Lee, Bhum-Cheol	Taejon		KR
Park, Kwon-Chul	Taejon		KR

US-CL-CURRENT: 710/241, 710/316

ABSTRACT:

A distributed type input buffer switch system includes at least one input data processing unit matched to an input port for storing and managing input data by target output ports, requesting arbitration for switching, and storing and managing information on an arbitration-requested data; an arbitration unit for managing an arbitration request signal received from the input data processing unit according to the input data processing unit and the target output port and performing arbitration according to an arbitration request; and a switching unit for receiving data from the input data processing unit and transmitting the same to the output ports by performing switching according to a command from the arbitration unit.

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Summary of Invention Paragraph - BSTX (10):

[0007] Accordingly, it is an object of the present invention to provide a distributed type input buffer switch system having arbitration latency tolerance and method for processing input data using the same which performs **arbitration for a request** generated irrespective of a transmission latency of request signals and grant signals by having a **double FIFO**(first-in-first-out) buffer at an input buffer and having a request FIFO buffer at a central arbiter.

US-PAT-NO: 6208644

DOCUMENT-IDENTIFIER: US 6208644 B1

TITLE: Network switch providing dynamic load balancing

DATE-ISSUED: March 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pannell; Donald Robert	Cupertino	CA	N/A	N/A
Hemming; Robert Donald	Ben Lomond	CA	N/A	N/A

US-CL-CURRENT: 370/389, 370/392 , 370/400 , 370/422

ABSTRACT:

A network switch routes data transmissions between network stations, each data transmission including network addresses of the source and destination network stations. The network switch includes a set of input/output (I/O) ports each for receiving data transmissions from and transmitting data transmissions to a subset of the network stations. Each I/O port is identified by a "physical" port ID and a "logical" port ID. While each I/O port's physical port ID is unique, all I/O ports that can route data to the same subset of network stations share the same logical port ID. Each I/O port receiving a data transmission from a network station sends its logical port ID and the network addresses included in the data transmission to an address translation system. The address translation system uses data in the translation request to maintain a lookup table relating each subset of network addresses to a logical port ID identifying all I/O ports that communicate with network stations identified by that subset of network address. The address translation system responds to an address translation request by returning the logical port ID of all I/O ports that can send data transmissions to a destination station identified by the destination address included in the data transmission. In response to the returned logical port ID, the network switch establishes a data path for the data transmission from the I/O port receiving the data transmission and any idle I/O port having that logical port ID.

10 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

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Brief Summary Text - BSTX (5):

Networks transfer data between computers or other types of network stations. For example 10BASE-T Ethernet systems use sets of twisted pair conductors to connect network stations to a **central** hub or **switch**. A network **switch** includes input ports for receiving data packets from various network sources, output ports for forwarding packets to various network destinations and a **switching** mechanism such as a crosspoint **switch** for selectively routing each incoming packet from an input port to the appropriate output port. The network **switch** also includes an address translation system which relates a network destination address included in each incoming packet to an output port that can forward the

packet to that network address. When an input port receives an incoming packet it stores the packet, reads its network destination address, consults the address translation system to determine which output port is to forward the packet, and then sends a routing **request to the switch's arbitration** system. When the **arbitration system determines that the requested** output port is idle it establishes a connection through the crosspoint **switch** between the requesting input port and the requested output port and then notifies the input port that it may begin sending the packet to the output port via the crosspoint **switch**.

US-PAT-NO: 6154799

DOCUMENT-IDENTIFIER: US 6154799 A

TITLE: Repeater-switch for distributed arbitration digital data buses

DATE-ISSUED: November 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gafford; Thomas Austin	Redondo Beach	CA	N/A	N/A
Eross, deceased; Botond Gabor	late of Palo Alto	CA	N/A	N/A
Moorer, legal representative;	San Rafael	CA	N/A	N/A
by James A.	San Rafael	CA	N/A	N/A
Barrie, legal representative;				
by Barbara L.				

US-CL-CURRENT: 710/107, 710/119

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed arbitration digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed arbitration buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed arbitration buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

13 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 8

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Brief Summary Text - BSTX (27):

Thus far, bus **switches** for arbitration type buses exist only for multi-master centralized arbitration buses. In such **central arbitration, requests for access to the bus come to a single arbitration** circuit. These **requests to the arbitration** circuit may be presented on several different bus

request signal lines that respectively correspond to different priority levels for the requesting devices. Multiple devices may be connected to the same wire-OR bus request signal line. When such bus **request signals arrive at the central arbitration** circuit, it decides when and to which priority level it will grant control of the bus. The result of the arbitration circuit's decision is then transmitted back to the devices via bus grant signal lines included in the bus. In these **central** arbitration buses, the bus grant signal lines are often daisy-chained through the devices connected to the bus so the first requesting device at a particular priority level can block retransmission of the grant signal to devices further along the bus from the **central** arbitration circuit, and thereby take control of the bus. This daisy-chaining and grant blocking, if present, is sometimes described a positional priority system.

Brief Summary Text - BSTX (28):

With these **central arbitration buses, since the bus request signals flow to the central arbitration** circuit and the bus grant signals flow from that circuit, it is relatively straight forward to build a bus **switch** that passes them between one of several sharing buses and the shared bus. By sensing whether the bus request signal and the bus grant signal pass through the **switch,** it can determine the proper direction to drive the bus control lines. Moreover, by sensing which of the two interconnected buses produces the data strobe signal and whether a read or write is occurring, the bus **switch** can decide in which direction to drive the data lines.